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(54) **Slew rate control and optimization of power consumption in a power stage**

Anstiegszeitsteuerung und Optimierung des Leistungsverbrauchs in einer Leistungsstufe

Commande du temps de montée et optimisation de la consommation d'un étage de puissance

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Description

[0001] The present invention relates to a method and relative driving circuit of an output power stage which permits an effective slew rate control and wherein current absorption by the driving circuitry is optimized in function of the operating conditions of the output power stage.

[0002] The so-called intelligent power switches are finding widespread industrial application. These devices permit to drive any kind of loads (capacitive, inductive and/or resistive), referred to ground (in a high-side driver configuration) or to the power supply voltage (in a low-side driver configuration). They are called "intelligent" because on a single chip are integrated circuits capable of protecting and regulating in a real time mode the state of the integrated power switch (for example to protect the integrated power device from a short circuit etc...).

[0003] At present, the most used technology for fabricating these integrated circuits is the so-called mixed of BCD technology (Bipolar-CMOS-DMOS). The integrated switch is often realized by a DMOS transistor, which, as compared with a bipolar transistor of similar current handling capacities, has the advantage of being voltage-driven, is capable of withstanding the maximum process voltage and has a lower saturation resistance.

[0004] On the other hand, in the field of industrial applications, the problem of electromagnetic disturbances that may be produced by continuous fast switchings of relays and equipments is very important. In order to minimize the electromagnetic noise that is produced, it is important to realize switches that are capable of ensuring suitably slow slew rates, in practice switching fronts having a controlled slope.

[0005] A common approach for switching-on and off a power transistor (power switch) with controlled switching front is that of loading and discharging the driving node of the transistor (the gate in the case of a field effect power transistor) with a constant current. Such a driving scheme, in case of a high-side driver employing a field effect power transistor (FET) is depicted in Figure 1.

[0006] EP-A-0 398 170 discloses a driver circuit for a power DMOST employing a differential amplifier that operates at a relatively low quiescent current when the DMOST is on. When the DMOST is to be switched from off to on, the differential amplifier tail current is briefly raised to a substantially higher value in order to quicken the charging of the parasitic capacitance of the gate of the driven DMOST. The tail current differential is determined by geometrically define IC quantities.

[0007] GB-A-2,257,854 discloses a drive circuit for an inductive load, wherein switch elements provide for a fast discharge path of the capacitor of the feedback differentiating circuit sensing the current flowing through the output load driver transistor

[0008] EP-A-0 326 968 discloses a driving circuit of a power transistor driving a load, were the slew rate of the output voltage of the driving circuit is controlled by modulating the output current of an op-amp of the circuit in function of the load as sensed by a feedback loop.

[0009] As well known to a skilled technician, such a solution does not permit to obtain perfectly controlled slew rates, because the slope of the switching front depends on the capacitance of the gate node which is not constant but assumes different values as the transistor passes from an off condition to a saturation condition and from the latter to a so-called linear working condition (i.e. an operating zone of its characteristic where the FET exhibits a resistive behaviour). Moreover, such a solution normally requires a circuitry capable of speeding up the passage from an off condition to a saturation condition at the beginning of a rising front and viceversa at the end of the descending front, and also for speeding up the passing from a saturation condition to a linear operating condition at the end of a rising front and viceversa at the beginning of a descending front, in order to maintain the turn-on and turn-off delays acceptably small.

[0010] An alternative approach used for controlling the slew rate is based upon the use of a high gain operational amplifier, configured as an integrating stage, employing a capacitor C in its feedback line, as shown in Figure 2.

[0011] Compared to the first solution, this alternative solution permits to obtain perfectly controlled switching fronts, because they are exclusively defined by the ratios between I_{ON}/C and I_{OFF}/C.

[0012] On the other hand, the operational amplifier must be provided with an output stage capable of driving the gate of the power FET (for example a DMOS transistor) which may have a parasitic capacitance of a value that may be as low as ten odd pF and as large as several thousands pF and a broad band in order to prevent oscillations.

[0013] Notwithstanding such a last approach may theoretically achieve a perfect slew rate control by suitably dimensioning the current generators I_{OFF} and I_{ON} and the bootstrap capacitance C (which may also be connected externally of the integrated circuit and therefore adapted according to need), it has the drawback of being unable to optimize also power consumption and the switching delays.

[0014] For these reasons, this solution is scarcely employed in systems and equipments where power consumption of the control circuitry represents a non negligeable aspect and destined to function at a relatively high switching frequency.

[0015] Moreover, in case of a power MOSFET, the driving must commonly be effected with a boosted voltage for reducing the resistance Ron of the power transistor. Therefore it is important that the current absorption from the supply node of the final stage of the driving operational amplifier, which is adequately boosted by employing a charge pump

circuit, be as slow as possible to avoid overloading the charge pump circuit.

[0016] Therefore there is the n ed and/or utility for an improved driving system which, beside allowing an easy slew rate control similar to that provided by a driving an integrating stage), also allows to optimize power consumption and to limit turn-on and turn-off delays.

[0017] This obj ctive is reached by the driving system of the invention which essentially consists in modulating the level of the current delivered by a driving operational amplifier and therefore current absorption, in function of different operating conditions of the output power transistor.

[0018] At the base of the invention, there is the recognition of the fact that the current required for suitably drive the output power transistor depends on the zone of its characteristic in which the power transistor is functioning.

[0019] In case of a MOSFET, when the transistor is completely on or off, the only current that is necessary to provide to its gate is just that sufficient to counterbalance the leakage and to ensure the actual state of the transistor (on or off).

[0020] During rising and descending switching phases, the current required is equal to about:

$$I = C_{GATE} \cdot \frac{V_S}{T}$$

where C_{GATE} is the capacitance seen from the gate node of the MOSFET, T represents the rise time or the fall time and V_S is the supply voltage of the circuit.

[0021] This current is such as to permit to the voltage swing of the output node to maintain a preset slope given by $I_{ON,OFF}/C$. Moreover, in order to speed up the passing from an off condition to a saturation condition, at the beginning of a rising front, and viceversa, at the end of a descending front, and also for speeding up the passage from a saturation condition to a "linear" condition, at the end of a rising front, and viceversa, at the beginning of a descending front, the current delivered by the driving amplifier should be suitably increased during these phases of the operating cycle of the power switch in order to reduce switching delays.

[0022] According to a first aspect of the invention which is defined by the claims, the current output by the driving operational amplifier and which is absorbed from the supply node of the final stage of the driving operational amplifier, is modulated as follows:

a) the current is minimum when the operational amplifier is completely unbalanced, a condition that occurs when the output power transistor is in a ON or in a OFF state;
b) the current is sufficient to ensure that the voltage on the output node of the circuit vary according to a preset slope for the entire duration of a rising or of a descending transition, during which the driving operational amplifier works in linear condition (under the control exerted by its own feedback loop) and the output power transistor is in saturation;
c) the current is maximum when the output power transistor crosses in one sense or in the other, the boundary between the OFF region and its "linear behaviour" region (resistive behaviour) of its characteristic and the value of which has an influence on the turn-on and on the turn-off delay times.

[0023] In practice, the system of the invention implements a modulation of the level of the current that is output by the driving operational amplifier in function of the operating conditions of a differential input stage of the operational amplifier itself, which reflect corresponding operating conditions of the output power transistor driven by the operational amplifier, as will be clearly explained and illustrated further on in this description.

[0024] The modulation of the driving current delivered by the operational amplifier to the control node of the power transistor is implemented by a special circuit capable of selecting among different bias conditions of the differential input stage (that is of current absorption), in function of the state of unbalance of the same differential input stage. The differential input stage may be a transconductance stage having a differential current output, and a plurality of current mirrors implement a final, single-ended stage which drives the output power transistor.

[0025] The different aspects and advantages of the invention will become more evident through the following description of several important embodiments and by referring to the attached drawings, wherein:

Figure 1 is a basic circuit diagram for the driving of an output power transistor (high-side driver) as described above;
Figur 2 is a basic circuit diagram for driving an output power transistor (high-side driver) by means of an integrating stage realized with a conventional operational amplifier, as described above;
Figure 3 shows a driving circuit for an output power transistor (high-side driver), made according to the present invention;
Figur 4 shows diagrams of the driving current delivered by the operational amplifier of Fig. 3;
Figure 5 shows diagrams of significant voltages of the circuit of Fig. 3, for an entire cycle of turning-on and turning-

off of the output power transistor;

Figure 6 shows an input circuit for a logic switching signal, suitable to reduce the turn-on and switching signal, suitable to reduce the turn-on and turn-off delay times;

Figure 7 is a diagram of the transfer function of the driving operational amplifier of Fig. 3, for a resistive load;

Figure 8 shows a driving circuit made according to the present invention for an output power transistor configured as a low-side driver.

[0026] A driving circuit according to the present invention for a power transistor PW_1, configured as a high-side driver, is depicted in Fig. 3.

[0027] Basically, a circuit of this type is capable of driving any type of load and the output node OUT of the circuit may also assume negative potentials (below ground). The latter characteristic is often required in driving heavy inductive loads (of several Henry), in order to speed up the demagnetization of the load. Without this specific requirement, the current mirror, *mirror3*, could be referred to the ground potential instead of the output node potential, as in the shown example.

[0028] The driving operational amplifier comprises three current mirrors (*mirror1*, *mirror2* and *mirror3*) which substantially form a final stage, and a differential input stage that is essentially composed of the differential pair of transistors N_1 and N_2 and the respective current generators I_Q.

[0029] The differential input stage of the operational amplifier is a transconductance stage with a differential current output (implemented through the drain currents of the transistors N1 and N2). The three current mirrors: *mirror1*, *mirror2* and *mirror3*, form a final stage of the operational amplifier, the single-ended output of which may be directly connected to the gate of the output power transistor PW_1, as shown.

[0030] Of course, the mirror ratios of the second and third current *mirrors: mirror2* and *mirror3*, which in the example shown are indicated as 1:10, may be of any suitable value, also a 1:1 ratio. Of course, a relatively large mirror ratio, as in the example shown, reduces current absorption in the differential input stage for the same level of output current.

[0031] According to the method of the present invention, the output current delivered by the driving operational amplifier is modulated in function of the state of operation of the circuit, by the circuit arrangement implemented with the transistors M_1 and M_2, the transistors P_1, P_2, P_3 and P_4 and with the auxiliary current generator I_M.

[0032] In general, all the current generators used in the circuit are not necessarily ideal generators but they are preferably realized with current mirror structures capable of delivering current as long as the voltage of their charge node remains close to the voltage to which they are referred (powered).

[0033] The transistors M_1 and M_2 are cross-coupled to the differential input pair of transistors of N_1 and N_2, and as the latter they are controlled by the signal present on the inverting input node in- of the operational amplifier and by the reference voltage V_R applied to the noninverting input in+ of the amplifier, respectively.

[0034] M_1 and M_2 have the function of limiting the output current of the driving operational amplifier to a level given by $2I_Q$, when the transconductance differential input stage is completely out of balance, that is when the signal present on the inverting input in- reaches ground potential or the potential $2V_R$.

[0035] In fact, when the voltage on the input node indrops below zero, the output transistor PW_1 is on and its gate is biased at the V_{CP} voltage, which may be a boosted voltage generated by a charge pump circuit (not shown in the figures). Commonly, in order to suitably overdrive a power MOSFET, the boosted voltage V_{CP} is about 10V higher than the supply voltage V_S, in order to optimize the internal resistance R_{DSon} of the power transistor. In these conditions of operation, the operational amplifier, that is its differential input stage, is completely out of balance.

[0036] In a state of full unbalance, in the above reiterated sense, of the differential input stage, the transistors M_1 and P_2 are on, while M_2, P_1, P_3 and P_4 are off. Therefore the transistor N_2, through its collector, absorbs from the boosted voltage node V_{CP} a current given by $2I_Q$. This condition persists for the full range of variation of the voltage on the inverting input node in- comprised between zero and the voltage V_{TH1}, given by:

$$V_{TH1} = V_R - V_{BE}(N_2) - V_{TH}(M_1)$$

where V_{TH1} is the threshold voltage of the transistor M_1.

[0037] A dual situation occurs when the output power transistor PW_1 is off. In this case, the inverting input in- of the driving operational amplifier is at the voltage $2V_R$. As a consequence M_2 and P_1 are on while M_1, P_2, P_3 and P_4 are off and in this case the transistor N_1 absorbs through its collector a current given by $2I_Q$. This condition persists for the whole range of values of the voltag on the inverting input node in- that are comprised between $2V_R$ and the voltage V_{TH2}, given by:

$$V_{TH2} = V_R + V_{BE}(N_1) + V_{TH}(M_2)$$

where V_{TH2} is th threshold voltage of the M_2 transistor.

[0038] Clearly the current generators I_Q may be sized so as to force a minimum current, that is a current that is just sufficient to compensate for dispersion currents of the gat node of the output power transistor PW_1 and therefore maintain a conducting state or a cut-off stat .

[0039] During a rising or descending transi nt (turn-on or turn-off of the power transistor), when the driving operational amplifier works in a linear manner, that is when the voltage on the inverting input node in- of the driving operational amplifier remains the vicinity of the reference voltage V_R, as diagrammatically depicted in Fig. 4, the feedback loop implemented by the capacitance C, assumes the control of the rise or fall slew rate thus ensuring a pre-established slope and the operational amplifier delivers the current that is necessary to charge or discharge the gate node of the output power transistor PW_1. In fact, in these conditions of operation, the collector currents $I_C(N_1)$ and $I_C(N_2)$ are tied to the voltages present on the inverting and on the noninverting inputs of the operational amplifier by the following trascendental relationships (corresponding to the exponential zones of the current diagrams of Fig. 4):

$$v(in) = V_T \cdot ln\left(\frac{I_C(N_1)}{I_C(N_2)}\right) + R_1 \cdot (I_C(N_1) - I_Q) + V_T \cdot ln\left(\frac{I_C(N_1) - I_Q}{I_Q}\right)$$

$$-v(in) = V_T \cdot ln\left(\frac{I_C(N_2)}{I_C(N_1)}\right) + R_2 \cdot (I_C(N_2) - I_Q) + V_T \cdot ln\left(\frac{I_C(N_2) - I_Q}{I_Q}\right)$$

[0040] At the beginning and at the end of a rise transient, respectively, the output power transistor passes from an off condition to a condition of linear operation and from the latter to a saturation condition. Similarly, at the beginning and at the end of a fall transient, the output power transistor passes from a saturation condition to a linear operation condition and from the latter to an off condition, respectively. During these phases, a relatively large charge or a discharge current of the driving node of the power transistor is required, for example in order to quickly reach the turn-on threshold V_{TH} of the power transistor on turning on and at the end of the turn-on transient, in order to quickly bring the V_{GS} voltage of the output power transistor to about 10V in order to optimize the resistance R_{DSon}.

[0041] According to the present invention, such a momentary requirement for a relatively high output current of the driving operational amplifier is satisfied by allowing the respective transistor of the differential pair of the input stage of the operational amplifier to absorb a markedly larger current than the curren $2I_Q$ that is fixed by the two current generators I_Q, through a dedicated auxiliary current generator I_M. This auxiliary current generator I_M is designed so as to force through the collector of the transistor that is conducting of the input differential pair of transistors, an additional current I_M, which is much greater than the current $2I_Q$ forced by the two current generators I_Q that bias the differential input stage. This is obtained by momentarily turning on one or the other of the two transistors P_3 and P_4, during a phase of relatively small unbalance of the differential input stage.

[0042] The explanation that follows will be more easily understood by referring also to the voltage diagram of Fig. 5.

[0043] In a turn-on phase of the output power transistor PW_1, the state of relatively small unbalance of the differential input stage of the operational amplifier coincides with the period during which the feedback loop of the operational amplifier is inactive, because the voltage on the gate node of the output power transistor has not yet risen above the turn-on threshold V_{TH}. As a consequence it is the transistor P_3 that turns on. Once the output voltage of the driving operational amplifier becomes greater than the threshold voltage V_{TH}, the output power transistor starts to conduct and therefore the feedback loop that controls the operation of the driving operational amplifier (the slew rate of the output voltage V_{out}) in the vicinity of the reference voltage V_R is activated for the duration of the rise transient.

[0044] At the end of the rise transient, that is when the output voltage V_{out} of the driving operational amplifier reaches the limit value, given by V_S+V_{GSon}, the voltage on the feedback capacitor C ceases to rise and also in this case the function of the feedback loop that controls the slope of the switching front (slew rate) ceases.

[0045] At this point, the transistor P_3 turns on again, thus allowing again the current forced by the driving operational amplifier (that is by the differential input stage) to rise to the maximum valu , given by I_M+2I_Q. In this way, the reaching of a full turn-on condition (overdrive) of the output power transistor is accelerated by quickly charging its control gate to the boosted voltage V_{CP}, which may be generated by a suitable charge pump circuit according to a common practice.

[0046] The turn-off of the output power transistor PW_1 occurs in a reverse manner.

[0047] Also in a turn-off phase, by the turning on of the transistor P_4, the maximum current given by the sum of: I_M+2I_Q, is forced by the driving operational amplifier during a discharge of the gate node of the output power transistor

from the overdrive voltage V_{CP} to the voltage given by V_S+V_{GSon}. At this point, the feedback loop that controls the slope of the fall front (slew rate) becomes active as long as the turn-off threshold V_{TH} of the output power transistor is overcome, which disactivates the f edback loop and causes again the turning-on of the transistor P_4 and thus the forcing by the driving operational amplifier of the maximum current until the voltage $2V_R$ is reached by the inverting input node V(in-).

[0048] By referring to Fig. 5, during a turn-on phase of the output power transistor PW_1, the delay T_1 corresponds to time necessary for the inverting input node (v(in-)) to discharge, because of the turning-on of the current generator I_{ON} and the turning-off of the current generator I_{OFF}, which are controlled by a pair of phase-opposed, logic signals (input and input\), during the drop of the v(in-) voltage from $2V_R$ down to V_R.

[0049] The delay T_2 represents the time necessary for the gate potential of the output power transistor to charge from ground potential up to a level beyond the turn-on threshold voltage V_{TH}.

[0050] It is this second contribution T_2 to the turn-on delay (and similarly also to the turn-off delay) that is advantageously reduced in the circuit of the invention by allowing the driving operational amplifier to deliver a relatively high current for quickly charging the gate node, during these phases.

[0051] Therefore the turn-on delay that is given by the sum of the delays T_1 and T_2 is markedly reduced. A similar reduction of the total delay time is achieved during a turn-off phase.

[0052] On the other hand, by analizing the first of the two delay factors, it may be observed that the time T_1 necessary for the inverting input of the operational amplifier to reach the reference voltage V_R (starting from $2V_R$ on turning-on or from 0 on turning-off) is given by:

$$T_1 = \frac{V_R \cdot C}{I_{ON,OFF}}$$

where C is the feedback capacitance that controls the slew rate.

[0053] Also such a first contribution to the switching delay (turn-off delay and turn-on delay) may be effectively reduced by employing a special input circuit as the one depicted in Fig. 6. By employing an input circuit as the one depicted in Fig. 6, the so optimized delay T_{1opt}, is given by the following expression:

$$T_{opt} = \frac{V_{BE} \cdot C}{I_{ON,OFF}}$$

[0054] In fact, with the input circuit of Fig. 6, the inverting input (in-) of the driving operational amplifier assumes istantaneously a V_{BE} voltage.

[0055] Therefore, beside optimizing the T_2 contribution to the turn-on delay (and to the turn-off delay), also the T_1 may be markedly reduced by employing an input circuit as the one depicted in Fig. 6.

[0056] Of course, it is important to ensure stability of the circuit. In the example shown, the mid-band gain of the feedback loop is given by:

$$G_0 = G_m \cdot R_G \cdot \frac{g_m \cdot R_L}{1 + g_m \cdot R_L}$$

where R_G is the resistance seen from the gate node, g_m is the transconductance of the output power transistor PW_1, R_L is the load resistance and G_m is given by the following relationship:

$$G_m = \frac{20}{\frac{2 \cdot V_T}{I_E} + R_1 + \frac{V_T}{I_E - I_Q}}$$

where I_E may be derived from th following trascendental relationship:

$$R_1 \cdot (I_E - I_Q) = V_T \cdot ln\frac{I_Q}{I_E - I_Q}$$

[0057] Resistances R_1 and R_2 of an appropriate value may be introduced (if necessary) in order to ensure stability of the circuit. Their effect is to make l ss steep the exponential rise and fall curves of the collector currents $I_C(N1)$ and $I_C(N2)$ in their r spective diagrams shown in Fig. 4.

[0058] Basically the feedback capacitor C introduces a "z ro" at the origin and a "pole" of valu $p_1=1/R_VC$, where R_V is the resistance seen by the capaciter C. The resistance R_V is given by the sum of two contributions. The load resistance of the circuit R_L (not shown in the circuit diagrams) and the resistance seen from the inverting node in- of the driving operational amplifier. Such a pole is the lowest because it is the one that determines the slew rate.

[0059] A second pole is introduced by the parasitic capacitance of the gate node of the output power MOSFET PW_1 and has a value given by $p_2=1/C_GR_G$. Other poles at higher frequencies are introduced by the operational amplifier. Therefore in designing the driving operational amplifier it is required that the pole p_2 remains dominant as compared with all the other poles.

[0060] For a purely resistive load, the transfer function is graphically depicted in Fig. 7.

[0061] Of course, if the load is not purely resistive, the poles and zeroes that are introduced concur to modify the transfer function and therefore it is necessary to verify that the stability requirements be satisfied, case by case.

[0062] Of course the invention may be applied also in the case of a configuration of the output power transistor as a low-side driver. Such an alternative embodiment of the invention is depicted in the circuit diagram of Fig. 8, for which the same considerations that have been made above for the case of a high-side driver configuration, hold.

[0063] According to preliminary CAD simulations, the driving circuit of the invention permits to readily achieve turn-on and turn-off delay of about 400 nanoseconds with a slew-rate of about 5V/µsec.

Claims

1. A method of switchingly driving an output stage constituted by a power transistor (PW_1) by way of a driving operational amplifier (I_Q, N_1, N_2, mirror1, mirror2, mirror3), **characterized in that** the slew rate of the voltage (OUT) on the output node of the output stage (PW_1) during rising and descending transients is controlled by

   modulating the level of the current ($I_c(N_1)$, $I_c(N_2)$) output by said driving operational amplifier in function of the passing from a condition of saturation to a condition of linear functioning of said transistor (PW_1) of the output stage as sensed by way of a feedback loop.

2. A driving method as defined in claim 1, wherein said transistor of the output stage is a field effect power (PW_1) transistor and the method comprises

   delivering a driving current of a preset minimum value (I_{OFF}) when said transistor (PW_1) is on or off and said driving operational amplifier is fully out of balance;
   delivering a driving current of a preset maximum value (I_{ON}) when said transistor passes, in either direction, from an off region to a linear operation region of its working characteristic and said operational amplifier is in a state of limited unbalance;
   delivering a driving current controlled by a feedback loop (C) of the operational amplifier so that the voltage of the output node (OUT) of the output stage varies with a preset slew rate during rising and descending t. ransients and while said field effect power transistor (PW_1) is in saturation.

3. A driving method according to claim 1, wherein the modulation of the level of the current ($I_C(N_1)$, $I_C(N_2)$) output by said driving operational amplifier is implemented by controlling the collector current of a transconductance, differential input stage (N_1, N_2, I_Q) of said driving operational amplifier I_Q, N_1, N_2, mirrorl, mirror2, mirror3).

4. A driving method according to claim 3, wherein during conditions of operation of said output stage that disable the control of the output current exerted by the feedback loop of the driving operational amplifier, the modulation of the level of the output current is realized by enabling and disabling an auxiliary current generator (I_M) forcing a certain current through the conducting transistor of said pair of transistors, depending on the state of unbalance of said differential input stage.

5. A driving circuit for an output stage, employing a driving operational amplifier comprising a transconductance, differential input stage (N_1, N_2, I_Q) and a current mirror final stage (mirrorl, mirror2, mirror3), **characteriz d by** comprising

   a feedback capacitor (C) connected between an output node (OUT) and an inverting input node (in-) of said differential input stage,

an auxiliary current generator (I_M) capable of forcing through the conducting one or a pair of input transistors (N_1, N_2) of the differential input stage a current markedly larger than the current forced by resp ctive biasing current generators (I_Q) of a pair of input transistors (N_1, N_2) of said differential input stage;
switching means (P_3, P_4) controll d by a second pair of transistors (M_1, M_2), cross-coupled with the inputs (in+, in-) of said differential input stage, capable of enabling and disabling current paths between each of said transistors (N_1, N_2) of said differential input pair and said auxiliary current generator (I_M).

6. A driving circuit as defined in claim 5, wherein the transistors (N_1, N_2) of said differential input pair are bipolar NPN transistors, each having a collector cornected to an input of a current mirror (mirror1, mirror2).

7. A driving circuit as defined in claim 6, wherein the transistors of said second pair (M_1, M_2) are field effect transistors, each having a gate connected to a respective input (in-, in+) of said differential input stage, a source connected to the emitter of the NPN transistor (N_2, N_1) of the other input and a drain connected in common to a respective current generator (I_Q) and to the base of a pair of PNP transistors (P_3, P_4), the first of which has a collector connected to said auxiliary current generator (I_M) and an emitter connected to the emitter of the NPN transistor (N_2) of said input (in+) while the other PNP transistor has a collector connected to said auxiliary current generator (I_M) and an emitter connected to the emitter of the other NPN transistor (N1)of said other input (in-).

8. A driving circuit according to claim 7, wherein between the emitter of the PNP transistors (P_3, P_4) of said pair and the emitter of the respective NPP input transistor there is a stabilizing resistance (R_1, R_2).

9. A driving circuit as defined in claim 5, **characterized by** comprising an input circuit ($2 \cdot V_R$, I_{OFF}, I_{ON}) for a switching logic signal ($\overline{input}$), composed of a complementary stage which comprises a first NPN transistor, a second n-channel field effect transistor, a third p-channel field effect transistor and a fourth bipolar PNP transistor, functionally connected in series with each other between a node maintained at a voltage ($2V_R$) that is twice the value of the reference voltage (V_R) that is supplied to the non inverting input (in+) of said driving operational amplifier and a common ground node, the base of said first NPN transistor and of said fourth PNP transistor being connected in common to said reference voltage (V_R), the switching logic signal ($\overline{input}$), being applied to the gates connected in common of said second and third field effect transistors, the emitters of which are connected in common to the non inverting input node (in-) of the driving operational amplifier.

Patentansprüche

1. Verfahren zum schaltbaren Ansteuern einer durch einen Leistungstransistor (PW_1) gebildeten Ausgangsstufe mittels eines Ansteuerungsoperationsverstärkers (I_Q, N_1, N_2, mirror1, mirror2, mirror3), **dadurch gekennzeichnet, daß** die Anstiegsgeschwindigkeit der Spannung (OUT) am Ausgangsknoten der Ausgangsstufe (PW_1) während der ansteigenden und absteigenden Einschwingvorgänge gesteuert wird durch
Modulieren des Pegels des Stroms ($I_C(N_1)$, $I_C(N_2)$), der von dem Ansteuerungsoperationsverstärker als Ant wort auf den Übergang von einem Zustand der Sättigung in einen Zustand des linearen Betriebs des Transistors (PW_1) der Ausgangsstufe, der durch eine Rückkopplungsschleife erfaßt wird, ausgegeben wird.

2. Ansteuerungsverfahren nach Anspruch 1, wobei der Transistor der Ausgangsstufe ein Feldeffekt-Leistungstransistor (PW_1) ist und das Verfahren umfaßt:

Liefern eines Treiberstroms mit einem im voraus festgelegten Minimalwert (I_{OFF}), wenn der Transistor (PW_1) durchschaltet oder gesperrt ist und der Ansteuerungsoperationsverstärker vollständig außer Gleichgewicht ist;
Liefern eines Treiberstroms mit einem im voraus festgelegten Maximalwert (I_{ON}), wenn der Transistor in irgendeiner Richtung aus einem Sperrbereich in einen Bereich mit linearem Betrieb seiner Betriebscharakteristik übergeht und der Operationsverstärker sich in einem Zustand mit begrenztem Ungleichgewicht befindet;
Liefern eines Treiberstroms, der durch eine Rückkopplungsschleife (C) des Operationsverstärkers gesteuert wird, so daß sich die Spannung des Ausgangsknotens (OUT) der Ausgangsstufe mit einer im voraus festgelegten Anstiegsgeswindigkeit während der ansteigenden und absteigenden Einschwingvorgänge ändert, während der Feldeffekt-Leistungstransistor (PW_1) gesättigt ist.

3. Ansteuerungsverfahren nach Anspruch 1, wobei die Modulation des P gels des Stroms ($I_C(N_1)$, $I_C(N_2)$), der von dem Ansteuerungsoperationsv rstärker ausgegeben wird, durch Steuern des Kollektorstroms einer differentiellen Transkonduktanz-Eingangsstufe (N_1, N_2, I_Q) des Ansteuerungsoperationsverstärkers (I_Q, N_1, N_2, mirror1, mirror2,

mirror3) ausgeführt wird.

4. Ansteuerungsverfahren nach Anspruch 3, wobei die Modulation des Pegels des Ausgangsstroms während Betriebszuständen der Ausgangsstufe, die die durch die Rückkopplungsschleife des Ansteuerungsoperationsverstärkers ausgeführte Steuerung des Ausgangsstroms verhindern, durch Fr igeben und Sperren eines Hilfsstromgenerators (I_M) erfolgt, der durch den leitenden Transistor des Transistorpaars in Abhängigkeit vom Zustand des Ungleichgewichts der differentiellen Eingangsstufe einen bestimmten Strom schickt.

5. Ansteuerungsschaltung für eine Ausgangsstufe, die einen Ansteuerungsoperationsverstärker verwendet, der eine differentielle Transkonduktanz-Eingangsstufe (N_1, N_2, I_Q) sowie eine Stromspiegel-Endstufe (mirror1, mirror2, mirror3) umfaßt, **gekennzeichnet durch**

   einen Rückkopplungskondensator (C), der zwischen einen Ausgangsknoten (OUT) und einen invertierenden Eingangsknoten (in-) der differentiellen Eingangsstufe geschaltet ist,
   einen Hilfsstromgenerator (I_M), der **durch** den leitenden Transistor eines Paars von Eingangstransistoren (N_1, N_2) der differentiellen Eingangsstufe einen Strom schickt, der deutlich größer als der Strom ist, der **durch** die jeweiligen Vorspannungsstromgeneratoren (I_Q) eines Paars von Eingangstransistoren (N_1, N_2) der differentiellen Eingangsstufe hindurchgeschickt wird;
   Schaltmittel (P_3, P_4), die **durch** ein zweites Paar Transistoren (M_1, M_2) gesteuert werden, die mit den Eingängen (in+, in-) der differentiellen Eingangsstufe kreuzgekoppelt sind und den Strompfad zwischen jedem der Transistoren (N_1, N_2) des differentiellen Eingangspaars und dem Hilfsstromgenerator (I_M) freigeben und sperren können.

6. Ansteuerungsschaltung nach Anspruch 5, wobei die Transistoren (N_1, N_2) des differentiellen Eingangspaars Bipolar-NPN-Transistoren sind, wovon jeder mit seinem Kollektor an einen Eingang des Stromspiegels (mirror1, mirror2) angeschlossen ist.

7. Ansteuerungsschaltung nach Anspruch 6, wobei die Transistoren des zweiten Paars (M_1, M_2) Feldeffekttransistoren sind, wovon jeder mit seinem Gate an einen entsprechenden Eingang (in-, in+) der differentiellen Eingangsstufe angeschlossen ist, mit seiner Source an den Emitter des NPN-Transistors (N_2, N_1) des anderen Eingangs angeschlossen ist und mit seinem Drain gemeinsam an einen jeweiligen Stromgenerator (I_Q) und an die Basis eines Paars PNP-Transistoren (P_3, P_4) angeschlossen ist, wobei der erste der beiden PNP-Transistoren mit seinem Kollektor an den Hilfsstromgenerator (I_M) und mit seinem Emitter an den Emitter des NPN-Transistors (N_2) des einen Eingangs (in+) angeschlossen ist, während der andere PNP-Transistor mit seinem Kollektor an den Hilfsstromgenerator (I_M) und mit seinem Emitter an den Emitter des anderen NPN-Transistors (N_1) des anderen Eingangs (in-) angeschlossen ist.

8. Ansteuerungsschaltung nach Anspruch 7, wobei zwischen dem Emitter der PNP-Transistoren (P_3, P_4) des Paars und dem Emitter des entsprechenden NPN-Eingangstransistors ein Stabilisierungswiderstand (R_1, R_2) geschaltet ist.

9. Ansteuerungsschaltung nach Anspruch 5, **gekennzeichnet durch** eine Eingangsschaltung ($2V_R$, I_{OFF}, I_{ON}) für ein Schaltlogiksignal ($\overline{\text{input}}$), die aus einer komplementären Stufe aufgebaut ist, die einen ersten NPN-Transistor, einen zweiten n-Kanal-Feldeffekttransistor, einen dritten p-Kanal-Feldeffekttransistor und einen vierten Bipolar-PNP-Transistor umfaßt, die zwischen einem Knoten, der auf einer Spannung ($2V_R$) gehalten wird, die gleich dem doppelten Wert der an den nichtinvertierenden Eingang (in+) des Ansteuerungsoperationsverstärkers angelegten Referenzspannung (V_R) ist, und einem gemeinsamen Masseknoten funktional in Reihe geschaltet sind, wobei die Basis des ersten NPN-Transistors und des vierten PNP-Transistors gemeinsam an die Referenzspannung (V_R) angeschlossen sind und das Schaltlogiksignal ($\overline{\text{input}}$) an die zusammengeschalteten Gates des zweiten und des dritten Feldeffekttransistors angelegt wird, deren Emitter gemeinsam an den nichtinvertierenden Eingangsknoten (in-) des Ansteuerungsoperationsverstärkers angeschlossen sind.

Revendications

1. Procédé pour piloter de façon commut´e un étage de sortie constitué d'un transistor de puissance (PW_1) au moyen d'un amplificat ur opérationnel pilote (I_Q, N_1, N_2, miroir1, miroir2, miroir3), **caract´risé en ce que** la vitesse de variation de la tension (OUT) sur le noeud de sortie de l'étage de sortie (PW_1) pendant les transitoires de montée

et de descente est commandée en modulant le niveau du courant ($I_C(N_1)$, $I_C(N_2)$) fourni par l'amplificateur opérationnel pilote en fonction du passage d'un état de saturation à un état de fonctionnement linéair (PW_1) de l'étage de sortie tel que détecté par une boucle de réaction.

2. Procédé selon la revendication 1, dans lequel le transistor de l'étage de sortie est un transistor de puissance à effet de champ (PW_1) et en ce que le procédé comprend les étapes suivantes :

   fournir un courant de commande de valeur minimum prédéterminée (I_{OFF}) quand le transistor (PW_1) est passant ou bloqué et que l'amplificateur opérationnel pilote est complètement déséquilibré ;
   fournir un courant de commande de valeur maximum prédéterminée (I_{ON}) quand le transistor passe, dans un sens ou dans l'autre d'une région bloquée à une région de fonctionnement linéaire de sa caractéristique de fonctionnement et que l'amplificateur opérationnel est dans un état de déséquilibre limité ;
   fournir un courant de commande déterminé par une boucle de réaction (C) de l'amplificateur opérationnel de sorte que la tension du noeud de sortie (OUT) de l'étage de sortie varie avec un taux de variation prédéterminé pendant les transitoires de montée et de descente et tandis que le transistor de puissance à effet de champ (PW_1) est en saturation.

3. Procédé selon la revendication 1, dans lequel la modulation du niveau du courant ($I_C(N_1)$, $I_C(N_2)$) fourni par l'amplificateur opérationnel pilote est mis en oeuvre en commandant le courant de collecteur d'un étage d'entrée différentiel à transconductance (N_1, N_2, I_Q) de l'amplificateur opérationnel pilote (I_Q, N_1, N_2, Miroir1, Miroir2, Miroir3,.

4. Procédé selon la revendication 3, dans lequel pendant des états de fonctionnement de l'étage de sortie qui invalident la commande du courant de sortie exercée par la boucle de réaction de l'amplificateur opérationnel pilote, la modulation du niveau du courant de sortie est réalisée en validant et en invalidant un générateur de courant auxiliaire (I_M) forçant un certain courant dans le transistor en conduction de la paire de transistors, selon l'état de déséquilibre de l'étage d'entrée différentiel.

5. Circuit de commande d'un étage de sortie utilisant un amplificateur opérationnel pilote comprenant un étage d'entrée différentiel à transconductance (N_1, N_2, I_Q) et un étage final de miroir de courant (miroir1, miroir2, miroir3), **caractérisé en ce qu**'il comprend :

   un condensateur de réaction (C) connecté entre un noeud de sortie (OUT) et un noeud d'entrée inverseur (in-) de l'étage d'entrée différentiel ;
   un générateur de courant auxiliaire (I_M) propre à forcer dans celui qui conduit d'une paire de transistors (N_1, N_2) de l'étage d'entrée différentiel un courant notablement plus grand que le courant forcé par le générateur de courant de polarisation respectif (I_Q) d'une paire de transistors d'entrée (N_1, N_2) de l'étage d'entrée différentiel ;
   un moyen de commutation (P_3, P_4) commandé par une seconde paire de transistors (M_1, M_2) connectés de façon croisée avec les entrées (in+, in-) de l'étage d'entrée différentiel propre à valider et invalider des trajets de courant entre chacun des transistors (N_1, N_2) de la paire d'entrée différentielle et du générateur de courant auxiliaire (I_M).

6. Circuit de commande selon la revendication 5, dans lequel les transistors (N_1, N_2) de la paire d'entrée différentielle sont des transistors bipolaires de type NPN ayant chacun un collecteur connecté à une entrée d'un miroir de courant (miroir1, miroir2).

7. Circuit de commande selon la revendication 6, dans lequel les transistors de la seconde paire (M_1, M_2) sont des transistors à effet de champ ayant chacun une grille connectée à une entrée respective (in-, in+) de l'étage d'entrée différentiel, une source connectée à l'émetteur du transistor NPN (N_2, N_1), de l'autre entrée et un drain connecté à un générateur de courant respectif (I_Q) et à la base d'une paire de transistors PNP (P_3, P_4) dont le premier a un collecteur connecté au générateur de courant auxiliaire (I_M) et un émetteur connecté à l'émetteur du transistor NPN (N_2) de l'entrée (in+) tandis que l'autre transistor PNP a un collecteur connecté au générateur de courant auxiliaire (I_M) et un émetteur connecté à l'émetteur de l'autre transistor NPN (N_1) de l'autre entrée (in-).

8. Circuit de commande selon la revendication 7, dans lequel, entre l'émetteur du transistor PNP (P_3, P_4) de la paire et l'émetteur du transistor d'entrée NPN respectif, est prévue une résistance de stabilisation (R_1, R_2).

9. Circuit de commande selon la revendication 5, **caractéris´ en ce qu**'il comprend un circuit d'entrée ($2 \cdot V_R$, I_{OFF},

I_{ON}), pour un signal logique de commutation ($\overline{input}$), constitu´ d'un étage complémentaire qui comprend un premier transistor NPN, un second transistor à effet de champ à canal N, un troisième transistor à effet de champ à canal P et un quatrième transistor bipolaire de type PNP, fonctionnellement connectés en série entre un noeud maintenu à une tension ($2V_R$) qui est égale à deux fois la valeur de la tension de référence (V_R) qui st fournie à l'entrée non inverseuse (in+) d l'amplificateur opérationnel pilote et un noeud de masse commun, les bases du premier transistor NPN et du quatrième transistor PNP étant connectées ensemble à la tension de référence (V_R), le signal logique de commutation ($\overline{input}$) étant appliqué aux grilles reliées ensemble des second et troisième transistors à effet de champ, les émetteurs étant connectés ensemble au noeud d'entrée non inverseur (in-) de l'amplificateur opérationnel pilote.

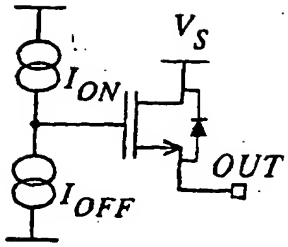

FIG. 1

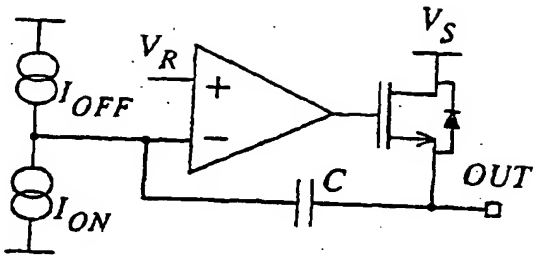

FIG. 2

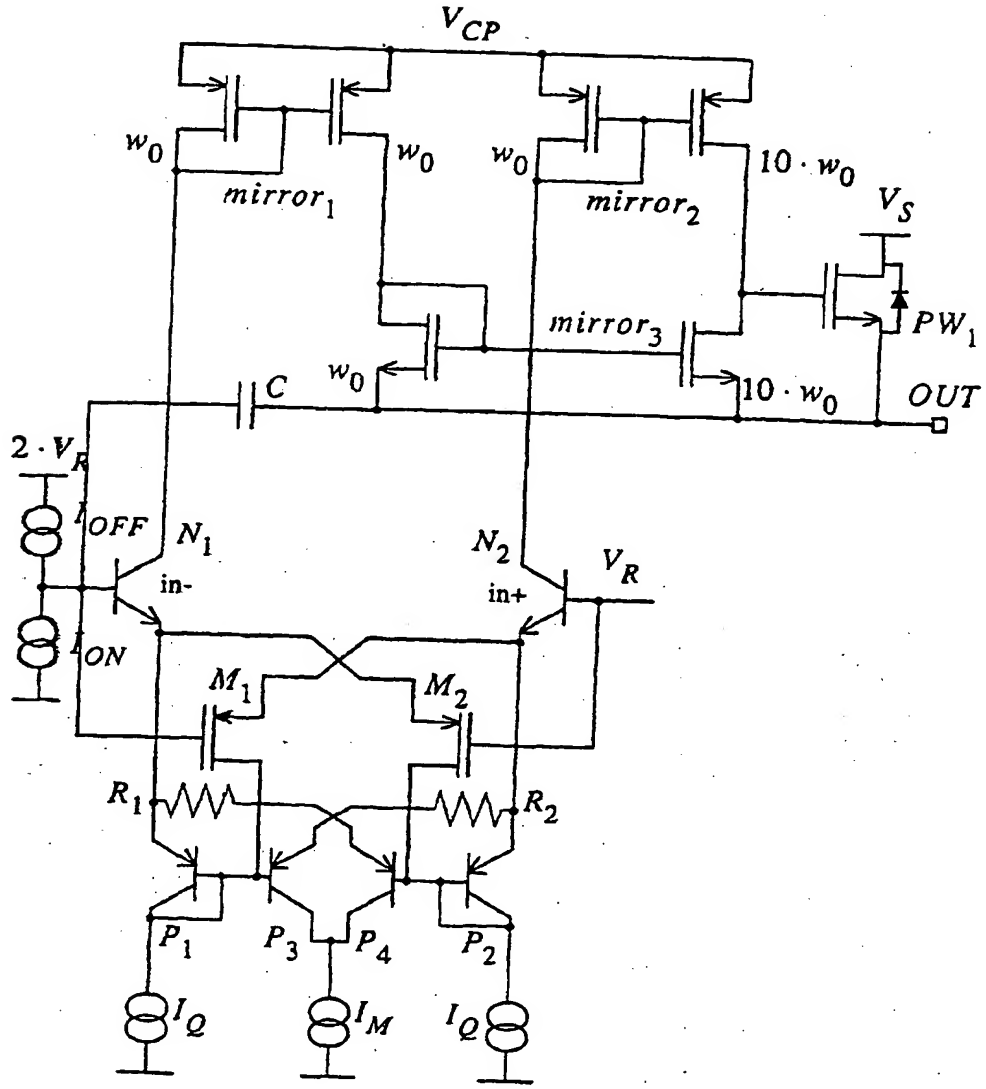

FIG. 3

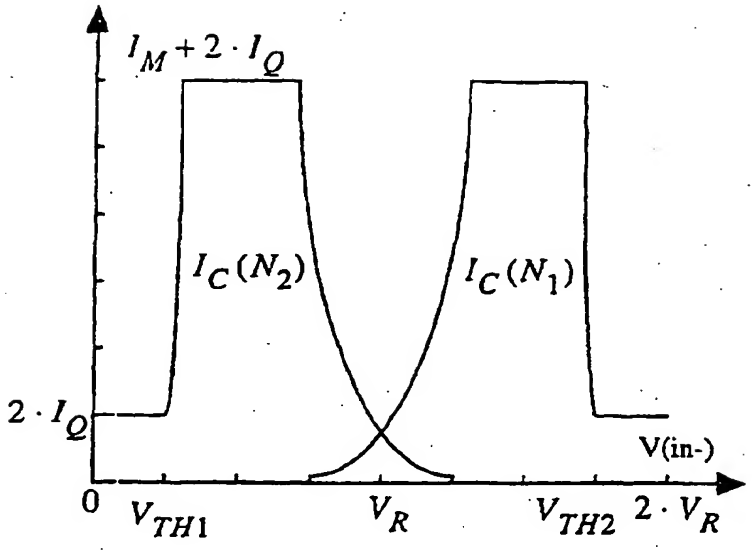
$I_M + 2 \cdot I_Q$
$I_C(N_2)$
$I_C(N_1)$
$2 \cdot I_Q$
V(in-)
0
V_{TH1}
V_R
V_{TH2}
$2 \cdot V_R$

FIG. 4

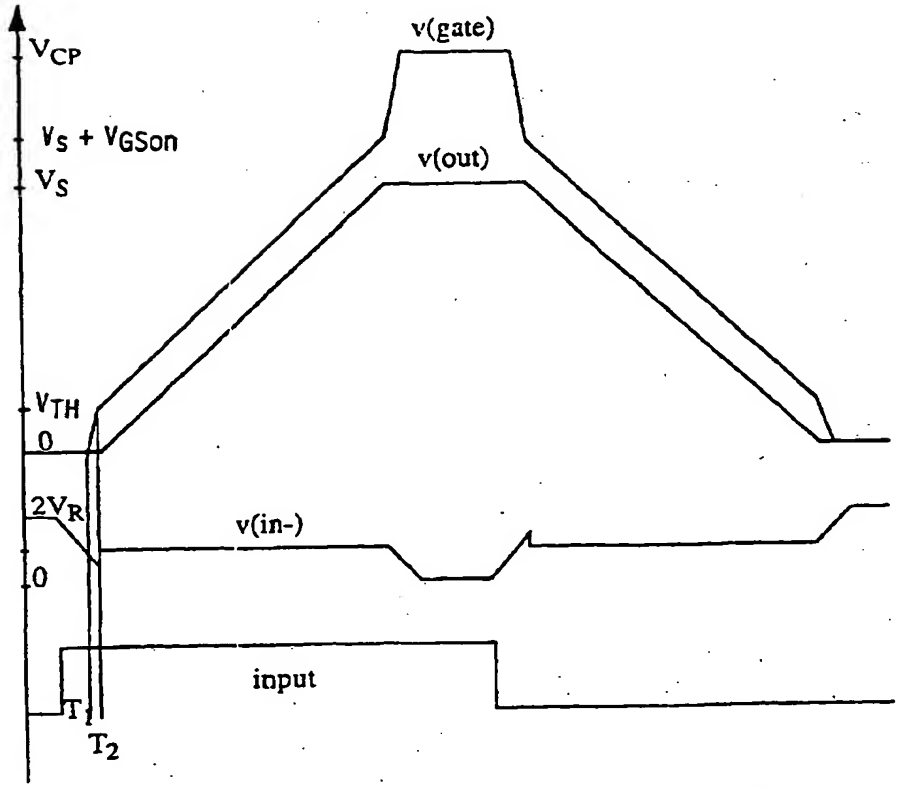
V_{CP}
$V_S + V_{GSon}$
V_S
v(gate)
v(out)
V_{TH}
0
$2V_R$
v(in-)
0
input
T_1
T_2

FIG. 5

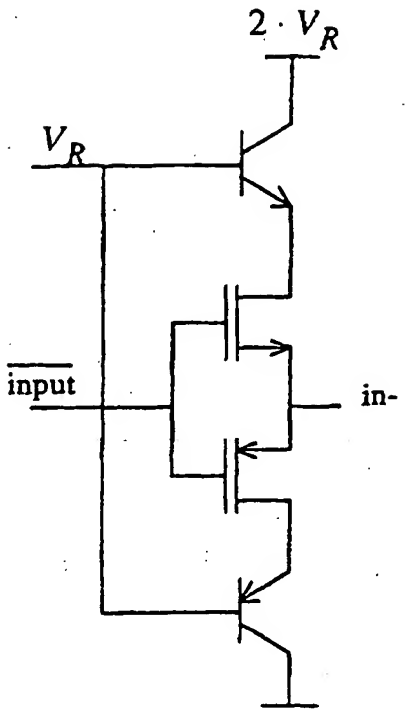

FIG. 6

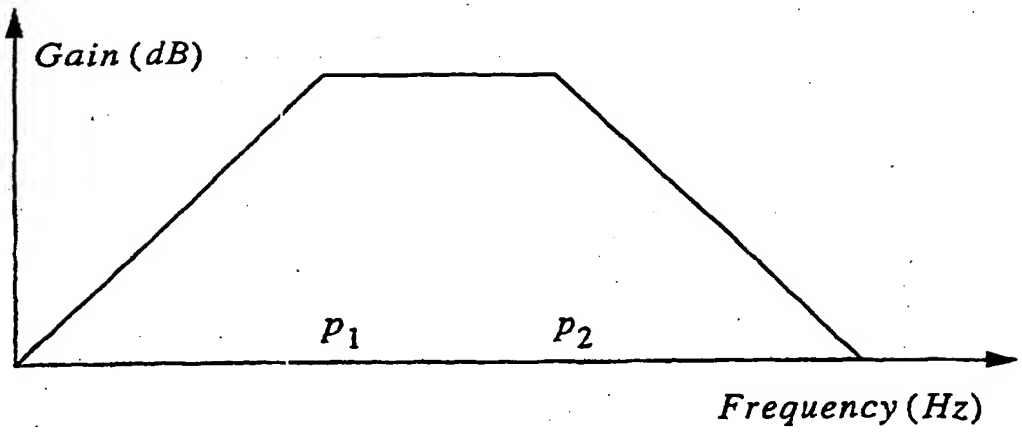

FIG. 7

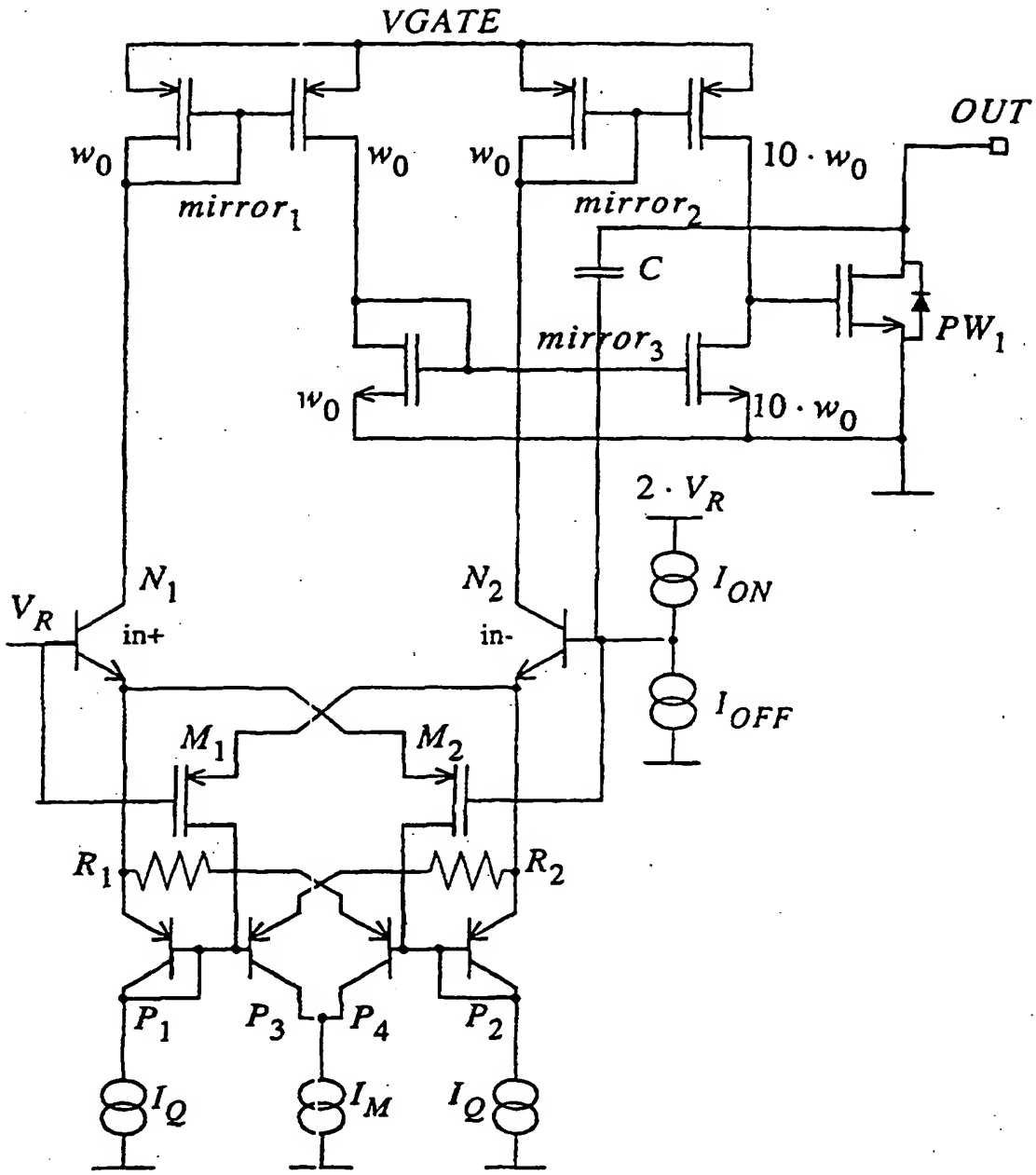
VGATE
OUT
w_0
w_0
w_0
$10 \cdot w_0$
$mirror_1$
$mirror_2$
C
$mirror_3$
PW_1
w_0
$10 \cdot w_0$
$2 \cdot V_R$
V_R
N_1
in+
N_2
in-
I_{ON}
I_{OFF}
M_1
M_2
R_1
R_2
P_1
P_3
P_4
P_2
I_Q
I_M
I_Q

FIG. 8